32Gb (2G x 16) DDR4 SDRAM

AS4C2G16D4 - 128 Meg x 16 x 16 Banks x 1 Ranks

Revision History

Revision	Details	Date
Rev 1.0	Initial Release	Sept. 2024

Description

The 32Gb Dual Die DDR4 SDRAM uses 16Gb DDR4 SDRAM die; two x8s combined to make one x16. It uses similar signals as the mono x16, and there is one extra ZQ connection for faster ZQ calibration and a BG1 control required for x8 addressing. Refer to Alliance's 16Gb DDR4 SDRAM data sheet (x8 option) for the specifications not included in this document.

Features

- Uses two x8 16Gb die to make one x16
- Single-rank DualDie
- $V_{DD} = V_{DDQ} = 1.2V$ (1.14–1.26V)
- 1.2V V_{DDQ}-terminated I/O
- JEDEC-standard ball-out
- Low-profile package

Features

- T_C = 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

Options — Marking

- Configuration
  - 128 Meg x 16 x 16 banks x 1 rank — 2G16
- 96-ball FBGA package (Pb-free)
  - 7.5mm x 13mm x 1.2mm
- Timing – cycle time[1]
  - 0.625ns @ CL = 22 (DDR4-3200) — -62
- Self refresh
  - Standard — None
- Operating temperature
  - Commercial (0°C ≤ T_C ≤ 95°C) — None

Table 1: Key Timing Parameters

Speed Grade[1]	Data Rate (MT/s)	Target CL-*n*RCD-*n*RP	^tAA (ns)	^tRCD (ns)	^tRP (ns)
-62	3200	22-22-22	13.75	13.75	13.75

Notes: 1. Refer to Speed Bin Tables for additional details.

Table 2: Ordering Information

Product part No	Org	Temperature Tc	Max Clock (MHz)	Package
AS4C2G16D4-62BCN	**2G x 16**	**Commercial 0°C to 95°C**	**1600**	**96-ball FBGA 7.5x13mm**

Table **3**: Addressing

Parameter	2048 Meg x 16
Configuration	128 Meg x 16 x 16 banks x 1 rank
Bank group address	BG[1:0]
Bank count per group	4
Bank address in bank group	BA[1:0]
Row addressing	128K (A[16:0])
Column addressing	1K (A[9:0])
Page size	1KB

Notes: 1. Page size is per bank, calculated as follows:
Page size = $2^{COLBITS} \times ORG/8$, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

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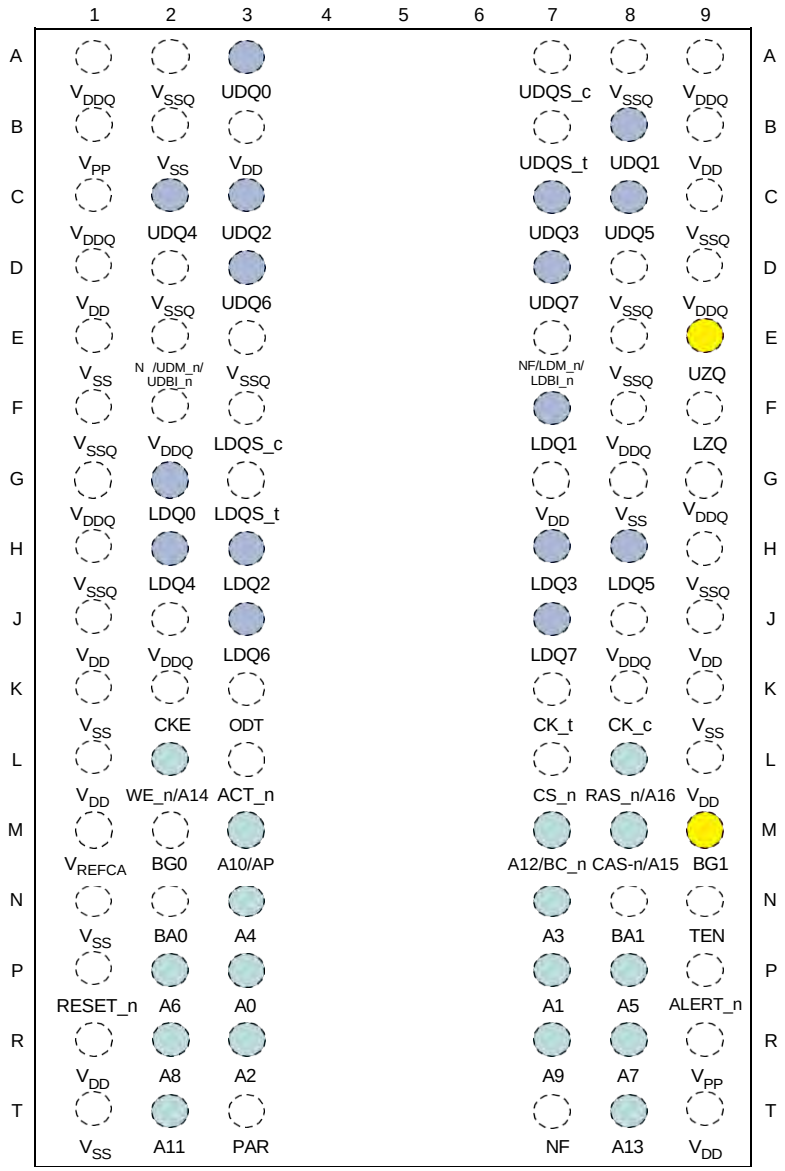
Ball Assignments

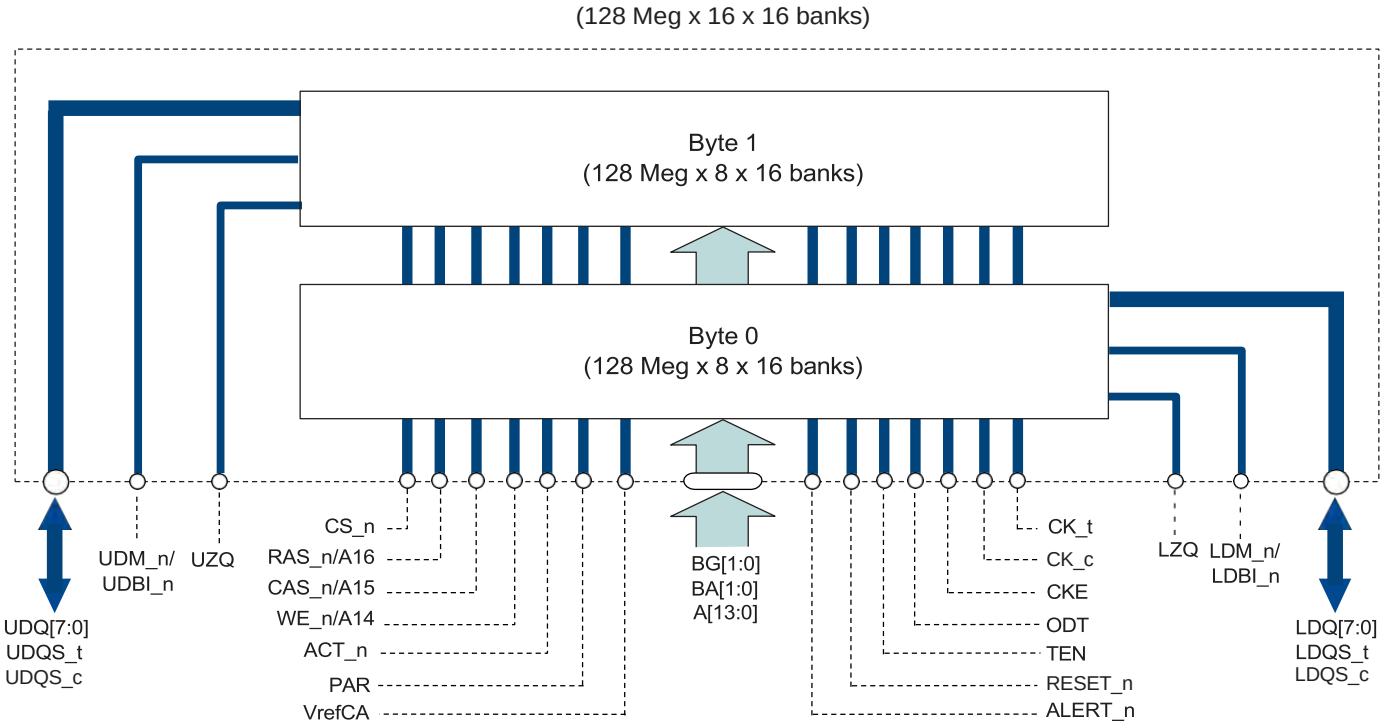
Figure 1: 96-Ball x16 SR DDP Ball Assignments



Notes: 1. See Ball Descriptions in the monolithic data sheet.
2. A slash "/" defines a mode register selectable function or command/address function. For example: Ball E2 = NF/UDM_n/UDBI_n where either NF, UDM_n, or UDBI_n is defined via MRS.

Functional Block Diagrams

Figure 2: Functional Block Diagram (128 Meg x 16 x 16 Banks x 1 Rank)



Connectivity Test Mode

Connectivity test (CT) mode for the x16 Dual Die single-rank (SR) device is the same as two mono x8 devices connected in parallel. The mapping is restated for clarity.

Minimum Terms Definition for Logic Equations

The test input and output pins are related by the following equations, where INV denotes a logical inversion operation and XOR a logical exclusive OR operation:

MT0 = XOR (A1, A6, PAR)
MT1 = XOR (A8, ALERT_n, A9)
MT2 = XOR (A2, A5, A13)
MT3 = XOR (A0, A7, A11)
MT4 = XOR (CK_c, ODT, CAS_n/A15)
MT5 = XOR (CKE, RAS_n/A16, A10/AP)
MT6 = XOR (ACT_n, A4, BA1)
MT7L = XOR (BG1, LDM_n/LDBI_n, CK_t)
MT7U = XOR (BG1, UDM_n/UDBI_n, CK_t)
MT8 = XOR (WE_n/A14, A12 / BC, BA0)
MT9 = XOR (BG0, A3, RESET_n and TEN)

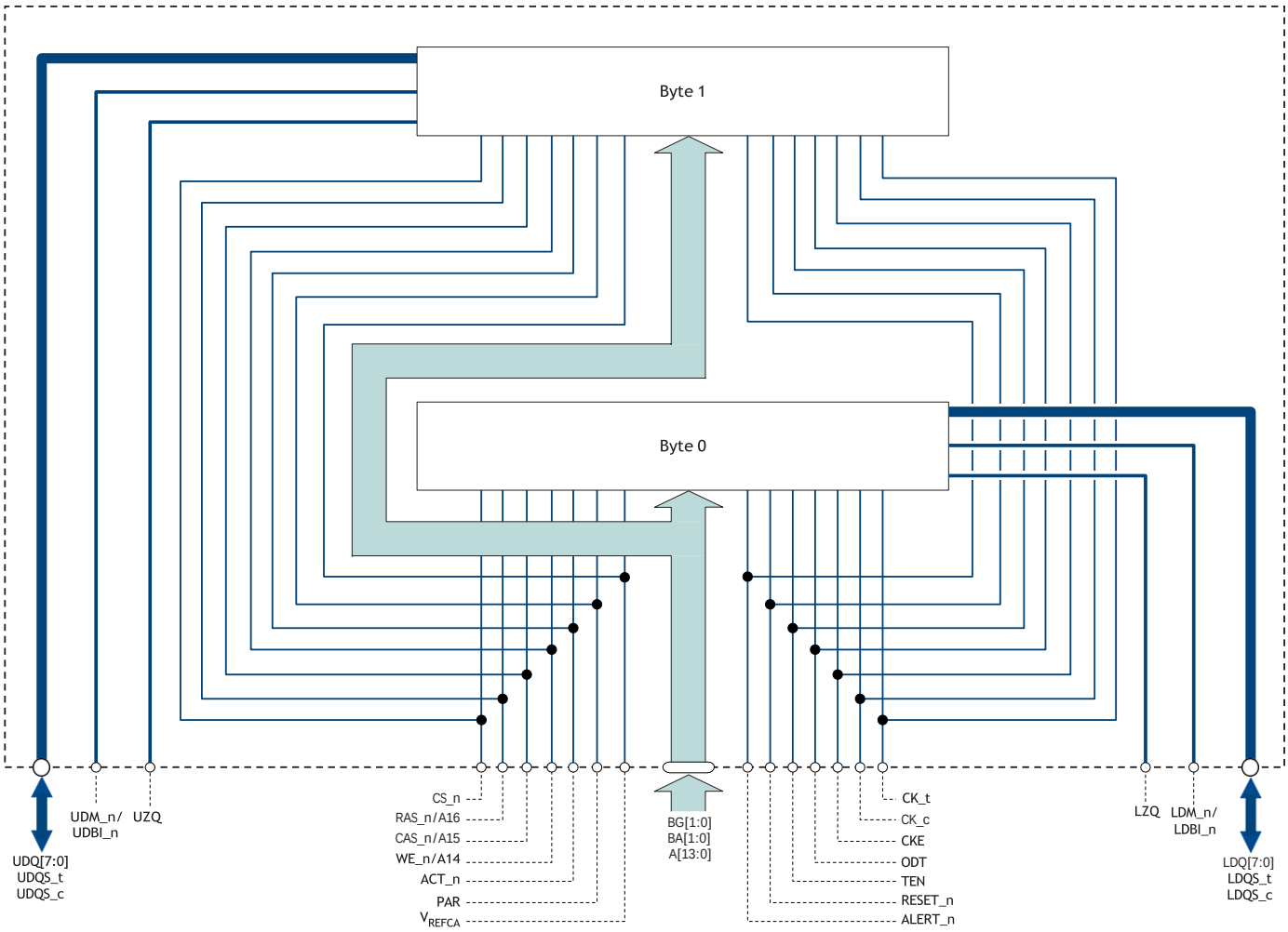
Logic Equations for a x16 **Dual Die**, SR Device

Byte 0	Byte 1
LDQ0 = MT0	UDQ0 = MT0
LDQ1 = MT1	UDQ1 = MT1
LDQ2 = MT2	UDQ2 = MT2
LDQ3 = MT3	UDQ3 = MT3
LDQ4 = MT4	UDQ4 = MT4
LDQ5 = MT5	UDQ5 = MT5
LDQ6 = MT6	UDQ6 = MT6
LDQ7 = MT7L	UDQ7 = MT7U
LDQS_t = MT8	UDQS_t = MT8
LDQS_c = MT9	UDQS_c = MT9

x16 **Dual** Die, SR Internal Connections

The figure below shows the internal connections of the x16 Dual Die, SR. The diagram shows why byte 0 and byte 1 outputs have the same logic equations except LDQ7 and UDQ7; they are different because the DM_n/DBI_n pins are not common for each byte.

Figure 3: x16 **Dual** Die, SR



Electrical Specifications - Leakages

Table 4: Input and Output Leakages

Symbol	Parameter	Min	Max	Units	Notes
I_I	Input leakage current Any input $0V \le V_{IN} \le V_{DD}$, V_{REF} pin $0V \le V_{IN} \le 1.1V$ (All other pins not under test = 0V)	-4	4	µA	1
I_{VREF}	V_{REF} supply leakage current $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)	-4	4	µA	2
I_{ZQ}	Input leakage on ZQ pin	-50	10	µA	
I_{TEN}	Input leakage on TEN pin	-12	20	µA	
I_{OZPD}	Output leakage: $V_{OUT} = V_{DDQ}$	-	10	µA	3 , 5
I_{OZPU}	Output leakage: $V_{OUT} = V_{SSQ}$	-50	-	µA	3, 4 , 5

Notes: 1. Any input 0V < Vin < 1.1V
2. $V_{REFCA} = V_{DD}/2$, V_{DD} at valid level.
3. DQs are disabled.
4. ODT is disabled with the ODT input HIGH.
5. This value needs to be multiplied by 2 for ALERT_n since it serves both bytes.

Temperature and Thermal Impedance

It is imperative that the DDR4 SDRAM device's temperature specifications, shown in the following table, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances listed in apply to the current die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Alliance technical note , "Thermal Applications," prior to using the values listed in the thermal impedance table. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The DDR4 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table **5**: Thermal Characteristics

Notes 1-3 apply to entire table

Parameter	Symbol	Value	Units	Notes
Operating temperature	T_C	0 to 85	°C	
		0 to 95	°C	4

Notes: 1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), if available, must be enabled.

Figure 4: Temperature Test Point Location

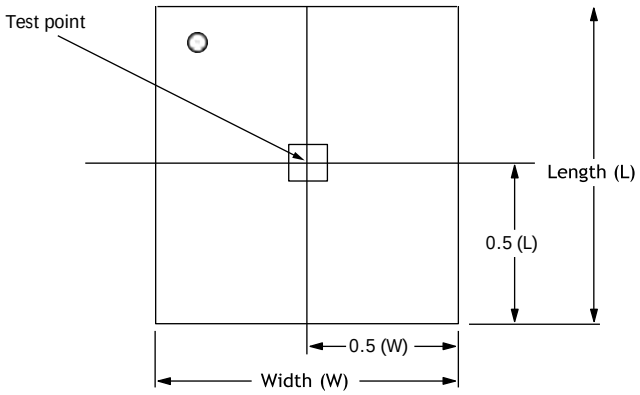


Table **6**: Thermal Impedance

Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)	Notes
96-ball	Low conductivity	48.7	36.9	32.4	NA	2.6	1
	High conductivity	28.7	23.7	22.0	9.7	NA	

Notes: 1. Thermal resistance data is based on a typical number.

DRAM Package Electrical Specifications

Table **7**: DRAM Package Electrical Specifications for x16 DDP Devices

Notes 1-2 apply to the entire table

Parameter		Symbol	DDR4-1600, 1866, 2133, 2400, 2666, 2933, 3200		Unit	Notes
			Min	Max		
Input/output	Zpkg	Z_{IO}	35	60	ohm	3
	Package delay	Td_{IO}	60	120	ps	3
	Lpkg	L_{IO}	-	5.5	nH	
	Cpkg	C_{IO}	-	4	pF	
DQSL_t/DQSL_c/DQSU_t/DQSU_c	Zpkg	$Z_{IO\ DQS}$	35	60	ohm	
	Package delay	$Td_{IO\ DQS}$	60	120	ps	
	Lpkg	$L_{IO\ DQS}$	-	5.5	nH	
	Cpkg	$C_{IO\ DQS}$	-	4	pF	
DQSL_t/DQSL_c, DQSU_t/DQSU_c,	Delta Zpkg	$DZ_{IO\ DQS}$	-	5	ohm	4
	Delta delay	$DTd_{IO\ DQS}$	-	5	ps	4
Input CTRL pins	Zpkg	$Z_{I\ CTRL}$	30	70	ohm	5
	Package delay	$Td_{I\ CTRL}$	60	120	ps	5
	Lpkg	$L_{I\ CTRL}$	-	7.5	nH	
	Cpkg	$C_{I\ CTRL}$	-	4	pF	
Input CMD ADD pins	Zpkg	$Z_{I\ ADD\ CMD}$	30	60	ohm	6
	Package delay	$Td_{I\ ADD\ CMD}$	60	120	ps	6
	Lpkg	$L_{I\ ADD\ CMD}$	-	7.5	nH	
	Cpkg	$C_{I\ ADD\ CMD}$	-	4	pF	
CK_t, CK_c	Zpkg	Z_{CK}	30	60	ohm	
	Package delay	Td_{CK}	60	120	ps	
	Delta Zpkg	DZ_{DCK}	-	5	ohm	7
	Delta delay	DTd_{DCK}	-	5	ps	7
Input CLK	Lpkg	$L_{I\ CLK}$	-	7.5	nH	
	Cpkg	$C_{I\ CLK}$	-	4	pF	
ZQ Zpkg		$Z_{O\ ZQ}$	-	50	ohm	
ZQ delay		$Td_{O\ ZQ}$	30	135	ps	
ALERT Zpkg		$Z_{O\ ALERT}$	30	60	ohm	
ALERT delay		$Td_{O\ ALERT}$	60	110	ps	

Notes: 1. The values in this table are guaranteed by design/simulation only, and are not subject to production testing.

2. Package implementations should satisfy targets if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown. The package design targets are provided for reference, system signal simulations should not use these values but use the Alliance package model.
3. Z_{IO} and Td_{IO} apply to DQ, DM, DQS_c, DQS_t, TDQS_t, and TDQS_c.
4. Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
5. $Z_{I\ CTRL}$ and $Td_{I\ CTRL}$ apply to ODT, CS_n, and CKE.
6. $Z_{I\ ADD\ CMD}$ and $Td_{I\ ADD\ CMD}$ apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, and WE_n.
7. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).

Current Specifications - Limits

Table **8**: DDR4 x16 **Dual** Die I_{CDD} and I_{CPP} Specifications and Conditions - ($0 \leq T_C \leq 85°C$)

Notes 1 and 2 apply to the entire table

Combined Symbol	Individual Die Status	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Units
I_{CDD0}	$I_{CDD0} = I_{DD0} * 2$	132	134	136	138	140	mA
I_{CPP0}	$I_{CPP0} = I_{PP0} * 2$	8	8	8	8	8	mA
I_{CDD1}	$I_{CDD1} = I_{DD1} * 2$	160	162	164	166	168	mA
I_{CDD2N}	$I_{CDD2N} = I_{DD2N} * 2$	82	84	86	88	90	mA
I_{CDD2NT}	$I_{CDD2NT} = I_{DD2NT} * 2$	108	110	112	114	116	mA
I_{CDD2P}	$I_{CDD2P} = I_{DD2P} * 2$	76	76	76	76	76	mA
I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} * 2$	84	84	84	84	84	mA
I_{CDD3N}	$I_{CDD3N} = I_{DD3N} * 2$	116	118	120	122	124	mA
I_{CPP3N}	$I_{CPP3N} = I_{PP3N} * 2$	4	4	4	4	4	mA
I_{CDD3P}	$I_{CDD3P} = I_{DD3P} * 2$	94	96	98	100	102	mA
I_{CDD4R}	$I_{CDD4R} = I_{DD4R} * 2$	282	308	334	360	386	mA
I_{CDD4W}	$I_{CDD4W} = I_{DD4W} * 2$	202	222	242	262	282	mA
I_{CDD5R}	$I_{CDD5R} = I_{DD5R} * 2$	136	136	136	136	136	mA
I_{CPP5R}	$I_{CPP5R} = I_{PP5R} * 2$	8	8	8	8	8	mA
I_{CDD6N}	$I_{CDD6N} = I_{DD6N} * 2$	106	106	106	106	106	mA
I_{CDD6_E}[3]	$I_{CDD6E} = I_{DD6E} * 2$	180	180	180	180	180	mA
I_{CDD6R}[3]	$I_{CDD6R} = I_{DD6R} * 2$	40	40	40	40	40	mA
I_{CDD6A} (25°C)[3]	$I_{CDD6A} = I_{DD6A} * 2$	22	22	22	22	22	mA
I_{CDD6A} (45°C)[3]	$I_{CDD6A} = I_{DD6A} * 2$	40	40	40	40	40	mA
I_{CDD6A} (75°C)[3]	$I_{CDD6A} = I_{DD6A} * 2$	102	102	102	102	102	mA
I_{CDD6A} (95°C)[3]	$I_{CDD6A} = I_{DD6A} * 2$	180	180	180	180	180	mA
I_{CPP6x}[3]	$I_{CPP6x} = I_{CPP6x} * 2$	12	12	12	12	12	mA
I_{CDD7}	$I_{CDD7} = I_{DD7} * 2$	400	400	400	400	400	mA
I_{CPP7}	$I_{CPP7} = I_{PP7} * 2$	26	26	26	26	26	mA
I_{CDD8}	$I_{CDD8} = I_{DD8} * 2$	72	72	72	72	72	mA

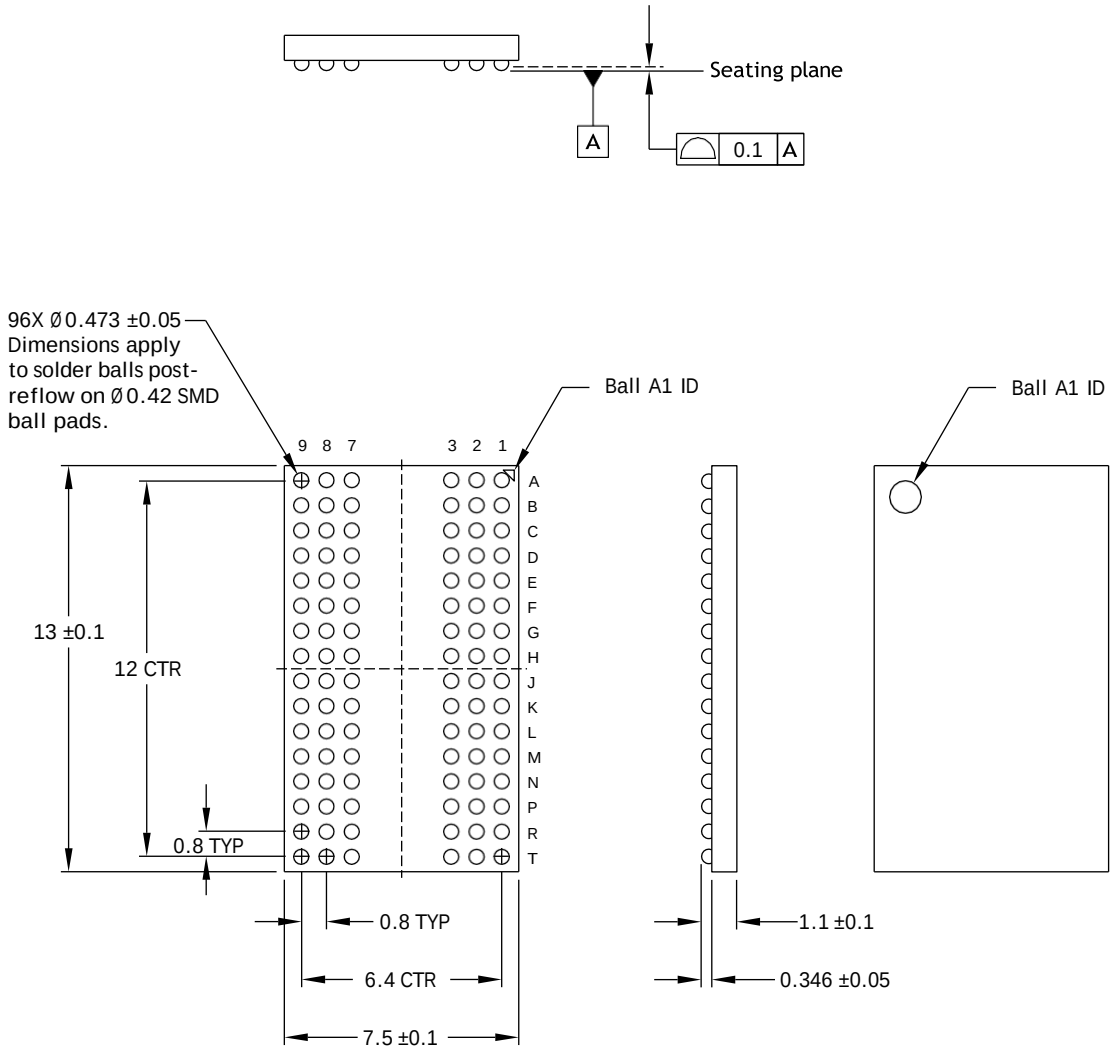
Notes: 1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.

2. I_{CDD} values must be derated (increased) when operated outside of the range $0°C \leq T_C \leq 85°C$. They must also be derated when using features such as CAL, CA parity, read/write DBI, AL, gear-down, write CRC, 2X/4X REF, and DLL disabled. Refer to the 16Gb monolithic data sheet for all derating values. Derating values apply to each individual I_{DDx} that make up the combined I_{CDD}.

3. I_{CDD6R} , I_{CDD6A}, and I_{CDD6E} values are verified by design and characterization, and may not be subject to production test.

Package Dimensions

Figure 5: 96-Ball FBGA



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SACQ (92.5% Sn, 4% Ag, 3% Bi, 0.5% Cu).

PART NUMBERING SYSTEM

AS4C	2G16D4	-62	B	C	N	XX
DRAM	2G16=2G x 16 D4=DDR4	62=1600 MHz	B=FBGA	C=Commercial temp 0°C~ 95°C	Indicates Pb and Halogen Free	Packing Type None:Tray TR:Reel

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